Fault Characterization And Testability Considerations Inmulti-Valued Logic Circuits

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Summary

With the growing interest and the emergence of various implementations of Multiple-Valued logic (MVL) circuits, testability issues of these circuits are becoming crucial. Fault characterization is an early step in the test generation process. It is aimed at finding fault models that best describe the possible faults expected to occur in a given class of circuits or technology. Layout and device level studies on CMOS and BiCMOS circuits revealed that the stuck-at model is not adequate to represent the actual physical defects. In this paper our aim is to characterize faults in a CMOS functionally complete set of MVL operators. The set has been implemented using existing standard binary CMOS technology. This enables us to characterize faults in these operators using the same techniques used for standard binary CMOS. Fault categories in MVL circuits and recommendations for testability will be given